REMARKS

Claims 1-34 are pending in this application. Claims 1 and 14 are independent. Claims 1, 2, 14 and 15 have been amended and claims 27-34 have been added.

Objection to the Specification

The specification has been objected to because the title is not descriptive. Accordingly, a new title has been included in this response. Applicants request that the objection to the specification be withdrawn.

Claim Objections

Claims 1, 2, 14, and 15 have been objected to for minor informalities. Claims 1, 2, 14, and 15 have been amended as recommended in the Office Action. Applicants request that the objection to the claims be withdrawn.

Claim Rejection – 35 U.S.C. § 102(b); Yoshikawa

Claims 1, 3-7, 9-12 have been rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent 6,335,554 (Yoshikawa). Applicants request reconsideration of the rejection based on the claims as amended.

The present invention relates to semiconductor memories consisting of a field-effect transistor capable of converting an electric charge variation to an electric current. The present

invention seeks to reduce thickness of known field-effect transistors capable of storing two or more bits, without substantial interference during two-bit operation.

Claim 1

The Office Action relies on Figures 1 and 2A to 2C of Yoshikawa for teaching elements of claim 1. Unlike the present invention, the memory cell structure of Yoshikawa includes two second gate electrodes 8 formed on an upper portion of a charge trapping layer 4. The first gate electrode 3 and the two second gate electrodes 8 are electrically connected to each other through a conductive layer 12.

In order to clarify this distinction, claim 1 has been amended to recite that the claimed semiconductor memory comprises "a single gate electrode" for a pair of charge storage sections. Applicants submit that at least for this reason the claimed semiconductor memory distinguishes over the memory cell structure of the first embodiment disclosed in Yoshikawa. Accordingly, Applicants request that the rejection be reconsidered and withdrawn.

Claim 3

Furthermore, claim 3 is directed to a semiconductor memory with first and second diffusion layer regions having an offset structure where the gate electrode does not overlap with the first and second diffusion layer regions. The Office Action only states that Figs. 1-2C of Yoshikawa discloses the claimed limitation.

Applicants submit that Yoshikawa does not disclose the limitation recited in claim 3. With regard to claim 1, the Office Action states that n-type diffusion layers 11 teach the claimed first n-type diffusion layer region and second n-type diffusion layer region. With respect to the n-

type diffusion layers 11 in the disclosure for Figs. 1-2C (discussed in col. 6, line 20, through col. 7, line 30), Yoshikawa states that,

> "An n-type diffusion layer 10 of a low impurity concentration adjacent to a channel area and an n-type diffusion layer 11 of a high impurity concentration located outside this n-type diffusion layer 10 are formed in the p-type semiconductor substrate 1 below this side wall spacer 9." (col. 6, lines 37-42).

Furthermore, the section concerning Figs. 1-2C mentions that the source and drain area are constituted by the n-type diffusion layers 10 of the low impurity concentration and the n-type diffusion layers 11 of the high impurity concentration. (col. 6, lines 48-54). No disclosure is made of an offset structure as required in claim 3. Thus, at least for this additional reason, Applicants submit that Yoshikawa fails to anticipate the feature recited in claim 3.

Claim 4

Similarly with respect to claim 4, Applicants submit that Yoshikawa fails to anticipate the feature of charge storage sections which overlap the channel region between the first n-type diffusion layer region and the second n-type diffusion layer region.

The Office Action indicates that the claimed charge storage sections are taught by Yoshikawa's charge trapping layers 4a, 4b. Yoshikawa discloses that charge trapping layers 4a, 4b are formed on both sides of the first gate electrode (col. 6, lines 29-30; lines 54-55). However, no disclosure is presented of the relationship between the extent of the charge trapping layers 4a, 4b and a channel region between the first and second diffusion layer regions, as required by claim 4.

Claim Rejection – 35 U.S.C. §103; Yoshikawa, Atsumi

Claim 2 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Yoshikawa in view of U.S. Patent 5,438,542 (Atsumi). Applicants respectfully traverse this rejection.

Claim 2 is directed to the semiconductor memory of claim 1 as well as that the p-type semiconductor film is set to a voltage less than the reference voltage. The Office Action admits that Yoshikawa fails to teach this claim limitation and instead relies on Atsumi for making up for this deficiency.

In particular, the Office Action states that Fig. 16 of Atsumi illustrates the claimed voltages. The Office Action states that it would have been obvious to one of ordinary skill in the art to utilize the collective data writing technique by means of substrate hot electrons of Atsumi in Yoshikawa's semiconductor memory "in order to improve the efficiency of injecting electrons and allow simultaneous data writing for a plurality of memory cells to reduce the time required for a erasing/writing cycle test and for data writing before data erasure." Applicants disagree.

Atsumi and Yoshikawa

Atsumi discloses a memory cell with a stacked gate structure and in particular, teaches a technique of hot electrons, while Yoshikawa discloses a semiconductor memory having a charge trapping layer for accumulating electrons that correspond to a plurality of bits. In Yoshikawa, writing is carried out by applying a high voltage to a diffusion region close to the charge trapping layer for accumulating electrons, while the region close to the other charge trapping layer is grounded. Such an application of voltage causes a channel hot electron to be generated and

captured in the charge trapping layer accumulating the electrons. (see Yoshikawa at column 7, lines 7-15). In Atsumi, collective data writing by means of substrate hot electrons is carried out with both source and drain voltages set at ground potential. Writing using substrate hot electrons occurs when electrons accelerated by a depletion layer between the substrate and the channel are made to jump over the barrier of the gate oxide film and inject into the floating gate (col. 8, lines 21-24).

At least because the substrate hot electron technique of Atsumi requires voltages of both the source and drain to be at ground potential, Applicants submit that applying the technique of Atsumi to the semiconductor memory having a charge trapping layer of Yoshikawa would render Yoshikawa unable to function to store charges in either charge trapping layer and store a plurality of bits. Accordingly, because of the substantial differences in structure and operation between teachings in Atsumi and Yoshikawa, Applicants submit that one of ordinary skill would not have been motivated to combine the teachings and the rejection thereby fails to establish *prima facie* obviousness. Applicants request that the rejection be reconsidered and withdrawn.

Claim Rejection – 35 U.S.C. § 103; Yoshikawa

Claims 8 and 14-25 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yoshikawa. Applicants request reconsideration of the rejection based on the claims as amended.

Claim 14

Similarly, as in the above for claim 1, claim 14 has been amended to clarify that the present semiconductor memory comprises a single gate electrode for a pair of charge storage

sections. Thus, the arguments as in the above for claim 1 apply as well to claim 14 and respective dependent claims. For at least this reason, Applicants request that the rejection be reconsidered and withdrawn.

In addition, the Office Action states that Yoshikawa discloses all the claimed limitations except for reversed impurities. Without any further evidence, the Office Action concludes that it would have been obvious to one of ordinary skill in the art at the time of the invention to reverse impurities to arrive at the claimed limitations as it involves only routine skill in the art. Because no evidence has been provided to support this conclusion, Applicants submit that the rejection fails to establish *prima facie* obviousness and request that the rejection be withdrawn.

Claim Rejection – 35 U.S.C. § 103; Yoshikawa, Eitan

Claims 13 and 26 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yoshikawa in view of Eitan. Applicants traverse this rejection.

At least for the reasons above for claim 1, applicable as well to claim 14, Applicants submit that the rejection fails to establish *prima facie* obviousness. Accordingly, Applicants request that the rejection be reconsidered and withdrawn.

New Claims

Claims 27 through 34 have been added. Claims 27-32 include additional features described in the present disclosure. Claims 33 and 34 recite specific values disclosed for the

offset region. Applicants submit that Yoshikawa fails to teach each and every feature of new claims 27-34.

Conclusion

In view of the above amendment, Applicants believe the pending application is in condition for allowance.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Robert W. Downs (Reg. No. 48,222) at the telephone number of (703) 205-8000, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Dated: September 22, 2005

Respectfully submitted,

By _____

RWD

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